

Fundamental Performance Limits of Carbon Nanotube Thin-Film Transistors Achieved Using Hybrid Molecular Dielectrics

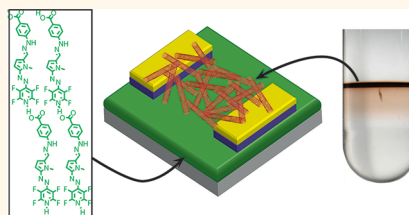
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Carbon nanotube (CNT) thin films¹ are promising semiconductors for diverse applications including large-area printed electronics,^{2–7} high-frequency devices,^{8,9} and light-emitting diodes.^{10,11} However, thin-film transistors (TFTs) fabricated from as-grown heterogeneous CNT films are intrinsically limited in performance due to contamination by metallic nanotubes.^{12–14} Furthermore, device performance is strongly constrained by gate dielectric details, including capacitive coupling to the channel, interfacial scattering, and trapped charges. To date, research efforts have largely focused on independent issues such as CNT purity,^{15–17} CNT density,^{5,18,19} channel geometry,^{2,20} and gate-dielectric properties^{3,21,22} to improve specific device metrics, often at the expense of others. More attractive for the ultimate incorporation of CNT films in low-power, large-area electronics is a more holistic approach whereby the gate dielectric and semiconductor channel are approached synergistically, resulting in simultaneous optimization of multiple device metrics, including important but less-discussed ones such as hysteresis.

The recent demonstration of scalable methods for producing monodisperse semiconducting CNTs^{15–17} offers immediate attractions and has afforded enhanced device performance such as large on/off ratios,⁶ large channel conductance,^{3,20} and high field-effect mobilities,^{7,17,18} together with large-area uniformity and yield.^{3,6,7} Moreover, minimization of metallic CNT content (<1%) permits use of thicker CNT films, which can sustain higher current densities in the on-state without significantly increasing the

ABSTRACT



In the past decade, semiconducting carbon nanotube thin films have been recognized as contending materials for wide-ranging applications in electronics, energy, and sensing. In particular, improvements in large-area flexible electronics have been achieved through independent advances in postgrowth processing to resolve metallic *versus* semiconducting carbon nanotube heterogeneity, in improved gate dielectrics, and in self-assembly processes. Moreover, controlled tuning of specific device components has afforded fundamental probes of the trade-offs between materials properties and device performance metrics. Nevertheless, carbon nanotube transistor performance suitable for real-world applications awaits understanding-based progress in the integration of independently pioneered device components. We achieve this here by integrating high-purity semiconducting carbon nanotube films with a custom-designed hybrid inorganic–organic gate dielectric. This synergistic combination of materials circumvents conventional design trade-offs, resulting in concurrent advances in several transistor performance metrics such as transconductance ($6.5 \mu\text{S}/\mu\text{m}$), intrinsic field-effect mobility ($147 \text{ cm}^2/(\text{V s})$), subthreshold swing (150 mV/decade), and on/off ratio (5×10^5), while also achieving hysteresis-free operation in ambient conditions.

KEYWORDS: density gradient ultracentrifugation · self-assembled nanodielectrics · nanoelectronics · mobility · transconductance · subthreshold swing

off-state current. While these thick CNT films can achieve higher current densities, the on/off ratios when using low-capacitance dielectrics are compromised due to CNT–CNT screening. Imperfections in the gate dielectric and/or suboptimal dielectric–CNT interfaces also degrade other key performance metrics such as hysteresis, threshold voltage, and subthreshold swing, properties

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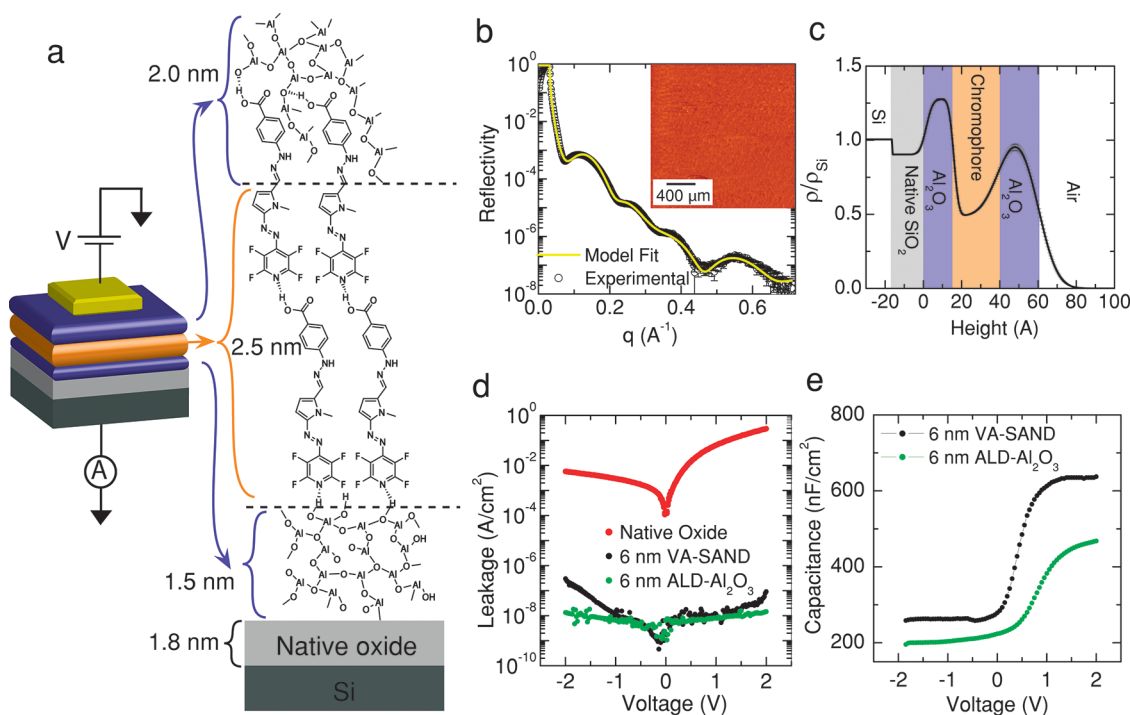


Figure 1. Structure and properties of VA-SAND gate dielectrics. (a) TFT schematic and chemical structure of VA-SAND on Si/SiO₂ substrates. (b) X-ray reflectivity data and best-fit results plotted as a function of the momentum transfer vector ($q = 4\pi \sin(2\theta/2)/\lambda$, where $2\theta =$ angle of the scattered X-rays and $\lambda =$ X-ray wavelength). Inset shows an AFM image of the VA-SAND surface with rms roughness = 0.65 nm. (c) Extracted electron density profile of VA-SAND, corresponding to best-fit results noted in (b), as a function of height from the native-oxide surface showing the densities of constituent layers. (d) Leakage current density of MIS fabricated on VA-SAND compared to that of 6 nm Al₂O₃ and native oxide on Si. (e) Capacitance of VA-SAND and 6 nm Al₂O₃ as a function of top-electrode voltage at 10 kHz.

that must be concurrently improved for effective implementation of low-power, high-speed CNT TFT-based electronics.

Toward this end, we report here the integration of >99% pure semiconducting CNTs with a new class of nanoscopic high-capacitance (630 nF/cm²) hybrid inorganic–organic gate dielectrics²³ to achieve TFT performance unconstrained by traditional trade-offs. The resulting devices simultaneously exhibit low operating voltages (4 V), low subthreshold swings (150 mV/decade), high normalized on-state conductance (8.5 μ S/ μ m), high normalized transconductance (6.5 μ S/ μ m), and high intrinsic field-effect mobilities (147 cm²/(V s)) with high on/off ratios (5×10^5) in ambient conditions. This unique combination of hybrid gate dielectrics with monodisperse semiconducting CNTs is compatible with low-temperature, large-area processing, thus offering applications in low-power TFT-based electronics. These devices also exhibit negligible hysteresis in transfer characteristics, unlike those fabricated with conventional oxide dielectrics, and avoid the ambipolarity that increases power consumption for CNT TFT circuits based on gel dielectrics.⁴ The hybrid dielectric (“VA-SAND”), fabricated by combining inorganic atomic layer deposition (ALD) with vapor phase organic self-assembly, can be grown with precise thickness control and combines layers of π -conjugated donor–acceptor building blocks,

self-assembled *via* hydrogen bonding ($\kappa \approx 9$),^{23,24} with ultrathin (~ 2 nm) layers of ALD-derived Al₂O₃ to enhance stability and dielectric characteristics (Figure 1a).

RESULTS AND DISCUSSION

Gate Dielectric Fabrication and Characterization. VA-SAND was grown on degenerately doped Si/SiO₂ substrates containing 1.8 nm thick native oxide (see Methods for details). VA-SAND microstructure and morphology were characterized by X-ray reflectivity (XRR) and AFM, while leakage current and capacitance–voltage (C – V) analysis were carried out on metal–insulator–semiconductor (MIS) capacitors. To highlight the differences between VA-SAND and purely inorganic oxide dielectrics grown by ALD, MIS capacitors and TFTs fabricated on ALD-grown Al₂O₃ (6-AO) of the same total thickness as VA-SAND (6 nm) were also characterized. The background-subtracted XRR data and model fits for VA-SAND on SiO_x are shown in Figure 1b. The electron density profile (normalized to the electron density of Si) resulting from the best fit of the XRR data using a 4-slab density model is plotted as a function of distance from the surface of the native oxide in Figure 1c.²⁵ The layer thicknesses are derived from the inflection points in the electron density profiles and are interpreted as the boundaries between layers.²⁶ The extracted thickness of the native oxide, the Al₂O₃ underlayer, the organic layer, and the Al₂O₃ capping

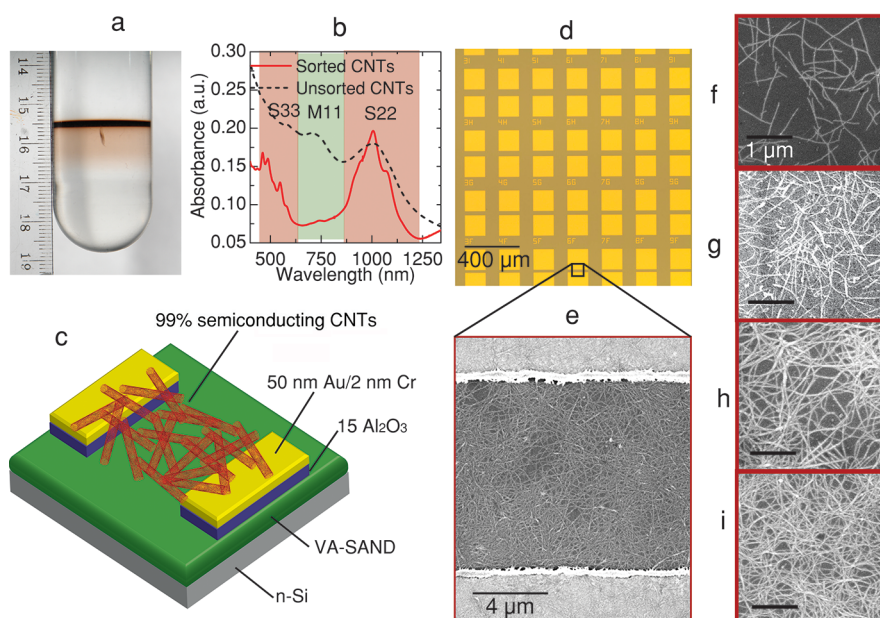


Figure 2. Architecture and channel morphology of CNT TFTs. (a) Optical micrograph of a centrifuge tube containing a 99% semiconducting CNT band after two iterations of density gradient ultracentrifugation. (b) Optical absorbance of sorted semiconducting CNTs compared with that of diluted unsorted CNTs to highlight semiconducting purity. Due to the different concentrations of CNTs in each solution, the absolute peak heights cannot be directly compared. (c) Schematic of a bottom-contact random CNT TFT fabricated on VA-SAND. (d) Optical micrograph of a large array of CNT TFTs with varying channel lengths. (e) Scanning electron microscopy (SEM) image of a CNT channel. (f–i) SEM images of CNT thin films with density-1, density-2, density-3, and density-4, respectively, as discussed in the text. Scale bars in f–i correspond to 1 μm .

layer are 1.8, 1.5, 2.5, and 2.0 nm, respectively. AFM images of VA-SAND (inset in Figure 1b) reveal an rms roughness of 0.65 nm, in agreement with the rms roughness of 0.7 nm extracted from the XRR analysis. Both VA-SAND and 6-AO exhibit comparable leakage current densities of 10^{-7} A/cm², up to 7 orders of magnitude lower than that of the SiO₂ native oxide as the top-electrode bias is varied from -2 V to 2 V (Figure 1d). Note that VA-SAND exhibits 37% higher capacitance (630 nF/cm²) than 6-AO (460 nF/cm²) with the substrate in accumulation ($V > 1.2$ V) due to the higher κ of the organic layer (Figure 1e). The capacitance decreases as the bias is varied from 1.2 V to -0.5 V due to the formation of the depletion region in the Si substrate and becomes constant for $V < V_{\text{th}} = -0.5$ V. VA-SAND also exhibits lower current leakage (10^{-7} A/cm²) and higher capacitance (630 nF/cm²) than previously reported vapor-deposited V-SAND²⁴ due to the reduced thickness combined with the higher κ of the robust upper inorganic layer (*vide infra*).

The dielectric constants of individual layers were determined by parallel plate capacitor analysis (see Methods) and were found to be 3.9, 6.0, 9.5, and 8.0 for the native oxide, the underlayer, the organic layer, and the upper capping layer, respectively. This thickness and dielectric constant analysis is consistent with the following observations: (1) the lower electron density (higher dielectric constant) of the capping layer *versus* the underlayer (Figure 1c); (2) the lower thickness of the organic layer (2.5 nm) compared to the length of

two head-to-tail hydrogen-bonded chromophore molecules (3.4 nm);²⁴ (3) the thicker upper capping layer (2 nm) *versus* that of the underlayer (1.5 nm) with the same number of ALD growth cycles; and (4) a rougher capping layer–organic layer interface *versus* ALD-grown Al₂O₃. These observations suggest significant intermixing of the chromophore and capping Al₂O₃ layers, yielding an effective dielectric constant of 8 for the intermixed capping layer, which is between 9.5 for the organic layer and 6.0 for Al₂O₃ (Figure 1a). Thus, intermixing explains the lower electron density, higher dielectric constant, and increased thickness and roughness of the capping layer. The net effective dielectric constant of a 6 nm thick VA-SAND layer (7.8 nm thick, including the native oxide) is found to be $\kappa_{\text{VA-SAND}} = 6.36$ (5.55). The effective oxide thickness of VA-SAND without (with) the native oxide is determined to be 3.68 nm (5.48 nm).

Carbon Nanotube Thin-Film Transistor Fabrication, Characterization, and Analysis. Figure 2a shows an optical micrograph of the semiconducting single-walled CNT band in a centrifuge tube after two iterations of density gradient ultracentrifugation (DGU) of arc-discharge-derived single-walled CNTs (Supplementary Section 1). The relative content of semiconducting CNTs is calculated to be 99% by comparing the relative area under the metallic and semiconducting peaks in the optical absorbance spectra, Figure 2b.^{15,17} Semiconducting CNT enrichment is clearly evident in the decreased (increased) metallic M11 (semiconducting S22 and S33)

peaks in the sorted CNT solution compared to the as-grown CNTs. Bottom-contact CNT TFTs were next fabricated on VA-SAND using photolithography (Methods) with channel lengths L varying from 5 to 50 μm and channel width $W = 100 \mu\text{m}$ (Figure 2c, d, e). The CNT average length was determined to be $1.36 \pm 0.92 \mu\text{m}$ from AFM analysis of a large ensemble of 334 nanotubes (Supplementary Section 2).

The origin of the resulting exceptional CNT/VA-SAND TFT performance is illustrated through a systematic analysis of device metrics at four different CNT film densities: density-1 = $5.5 \pm 0.9 \text{ CNTs}/\mu\text{m}^2$; density-2 = $13.3 \pm 1.7 \text{ CNTs}/\mu\text{m}^2$; density-3 = $22.7 \pm 1.9 \text{ CNTs}/\mu\text{m}^2$; and density-4 = $27.1 \pm 2.5 \text{ CNTs}/\mu\text{m}^2$ (Figure 2f–i). These CNT TFTs exhibit p-type behavior in ambient at low biases of $V_g = -2$ to 2 V and $V_d = -0.1$ V (Figure 3a,b). The negligible hysteresis of these TFTs on VA-SAND compared to that on 6-AO (Figure 3a and b) suggests significantly lower VA-SAND trap charge densities and/or favorably modified surface properties compared to the conventional oxide ALD dielectric of the same thickness. Note that the present CNT/VA-SAND devices exhibit small threshold voltages (<1 V) and ultralow subthreshold slopes, as low as ~ 100 mV/decade, compared to the quantum limit of ~ 70 mV/decade at room temperature (Supporting Figure S4b), making these TFTs suitable candidates for low-power, high-speed circuits. Note that the subthreshold slope as well as off-current (I_{off} , within the noise level of the instrumentation ~ 10 pA) remain relatively independent of drain bias (Figure 3c).

We next assess device parameters that underlie the performance of digital circuit building blocks such as inverters and ring oscillators.^{12,13} First, high field-effect mobility (high transconductance) is necessary to achieve large voltage gain inverters in high-speed circuits. Second, a low operating voltage and high on/off ratio (*i.e.*, low off-current) are necessary to minimize power dissipation. Finally, a reduced channel area (*i.e.*, high current capacity or normalized conductance) is desired to minimize parasitic capacitance in high-frequency digital circuitry. Note that while individual CNTs have large current-carrying capacities and high field-effect mobilities,²⁷ the effective field-effect mobility of CNT films is significantly reduced due to additional resistance from CNT–CNT junctions. Further reduction in the *estimated mobility* can result from assumptions made about the morphology of percolating CNT films in calculating the gate capacitance. There are two methods commonly used to estimate the capacitance of a random network CNT film. In the first, the CNT film is assumed to be continuous in a parallel plate geometry, affording a capacitance $C_g = C_{\text{PP}} = \epsilon_{\text{ox}}/t_{\text{ox}}$ ($630 \text{ nF}/\text{cm}^2$), where ϵ_{ox} and t_{ox} are the dielectric constant and thickness of the gate dielectric, respectively. Note that the assumed gate capacitance of $630 \text{ nF}/\text{cm}^2$ is the upper limit of the capacitance of

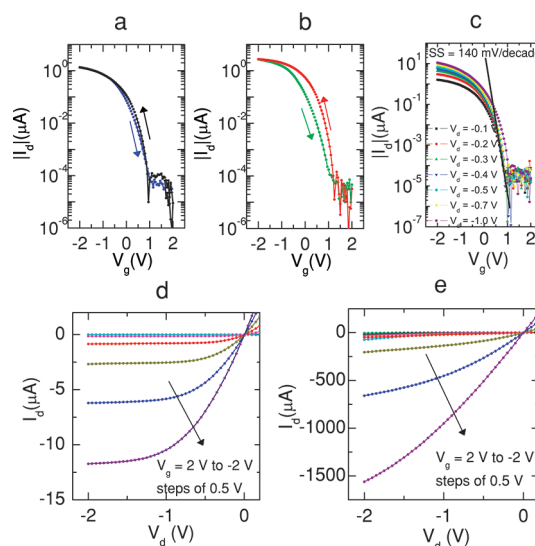


Figure 3. Transfer and output characteristics of CNT TFTs. (a) Transfer characteristics of a density-1 CNT TFT ($L = 5 \mu\text{m}$, $W = 100 \mu\text{m}$) on VA-SAND with forward and backward sweeps showing negligible hysteresis. (b) A density-1 CNT TFT ($L = 5 \mu\text{m}$, $W = 100 \mu\text{m}$) on 6 nm Al_2O_3 showing increased hysteresis. (c) Transfer characteristics of the same device as in (a) on VA-SAND showing low subthreshold slope (140 mV/decade) for drain bias (V_d) varying from -0.1 V to -1 V. (d and e) Output characteristics of CNT TFTs ($L = 5 \mu\text{m}$, $W = 100 \mu\text{m}$) with lowest CNT density ($5.5 \text{ CNTs}/\mu\text{m}^2$) and highest CNT density ($27.1 \text{ CNTs}/\mu\text{m}^2$).

VA-SAND at the onset of the inversion region ($V_{\text{top electrode}} = 1$ V for an MIS capacitor on n-type Si (Figure 1e) and $V_g = -1$ V for CNT TFTs). Thus, the reported field-effect mobilities actually underestimate the actual values. The second method takes into account electrostatic coupling between CNTs as well as the quantum capacitance of CNTs^{2,28} to obtain the intrinsic capacitance of the CNT films, C_{IN} . The dependence of C_{IN} on CNT density and gate-dielectric capacitance is illustrated in Supporting Section 4. Overestimation of capacitance in C_{PP} is more critical in the case of sparse CNT networks and high-capacitance gate dielectrics. For completeness, we report both the parallel-plate field-effect mobility (μ_{PP}) and intrinsic field-effect mobility (μ_{IN}) calculated from C_{PP} and C_{IN} , respectively, using $\mu = (L/C_g V_d W)(\partial I_d / \partial V_g)$, where I_d , V_d , and V_g are drain current, drain voltage, and gate voltage, respectively.

Figure 3d and e show the output characteristics of a low-density (density-1) and a high-density (density-4) CNT/VA-SAND TFT ($L = 5 \mu\text{m}$ and $W = 100 \mu\text{m}$), and Figure 4a compares the transfer characteristics of four different CNT density TFTs having the same channel dimensions. The drain current is varied over 2 orders of magnitude to determine the CNT density for optimum device performance. At all densities, the CNT TFTs show linear behavior at low V_d , suggesting ohmic CNT–electrode contacts. Since width-normalized on-state conductance ($G/W = I_d/(V_d W)$) is a commonly used figure-of-merit for current-carrying capacity, both G/W and I_d (at $V_d = -100$ mV) are plotted in linear and

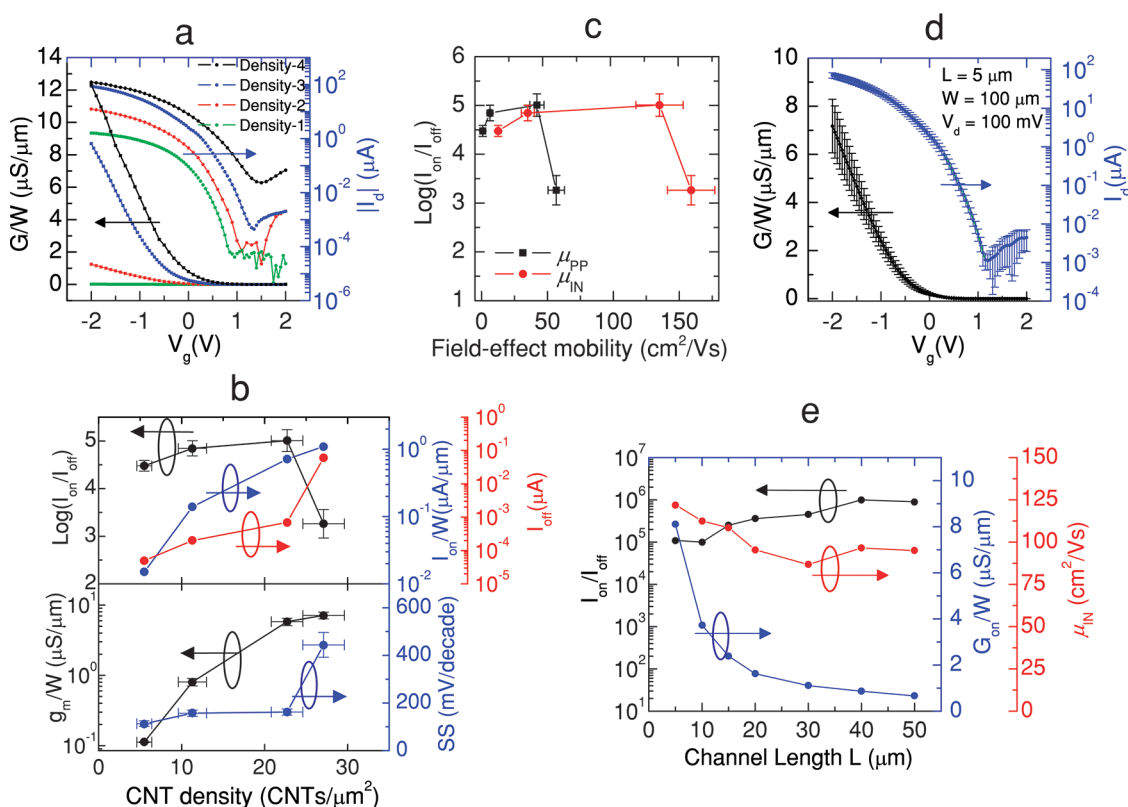


Figure 4. CNT density- and channel geometry-dependent characteristics of CNT/VA-SAND TFTs. (a) Transfer characteristics showing width-normalized conductance ($G/W = I_d/(V_d W)$) and drain current (I_d) of four CNT TFTs ($L = 5 \mu\text{m}$, $W = 100 \mu\text{m}$) with CNT density varying from density-1 (5.5 CNTs/ μm^2) to density-4 (27.1 CNTs/ μm^2). (b) Average device parameter normalized on-current I_{on}/W , off-current I_{off} , log of on/off ratio ($\log(I_{\text{on}}/I_{\text{off}})$), normalized transconductance $g_{\text{m,nor}}$, and subthreshold slope (SS) plotted as a function of CNT density for CNT TFTs from (a). Horizontal and vertical error bars represent standard deviation in CNT density and exponent m of on/off ratio (10^m), respectively. (c) $\log(I_{\text{on}}/I_{\text{off}})$ plotted as a function of field-effect mobility (see text) for four different CNT densities. $\log(I_{\text{on}}/I_{\text{off}})$ and field-effect mobility are averaged over five devices. (d) Average transfer characteristics of seven density-3 (22.7 CNTs/ μm^2) CNT TFTs ($L = 5 \mu\text{m}$, $W = 100 \mu\text{m}$). (e) Device parameters, on/off ratio, normalized on-state conductance (G_{on}/W), and intrinsic field-effect mobility (μ_{IN}) of density-3 CNT TFTs as a function of channel length L varying from $L = 5$ to $50 \mu\text{m}$ ($W = 100 \mu\text{m}$).

semilog plots, respectively (Figure 4a). The lowest CNT density (density-1), 5.5 CNTs/ μm^2 , is above the percolation threshold²⁹ $\rho_{\text{th}} = 4.24^2/\pi L_{\text{CNT}}^2 = 3.09$ CNTs/ μm^2 (average CNT length $L_{\text{CNT}} = 1.36 \mu\text{m}$), while the highest CNT density (density-4), 27.1 CNTs/ μm^2 , exhibits a low on-state sheet resistance (at $V_g = -2$ V) of 16.8 k Ω /square. The present CNT TFTs show dominantly p-type behavior with gradually increasing ambipolarity and larger I_{off} ($I_{\text{off}} = \text{minimum } I_d$) at higher CNT densities. Ambipolar behavior in thicker CNT films may reflect band-to-band tunneling due to increased fractions of small-diameter CNTs³⁰ and/or decreased interaction of CNTs with adsorbates in thicker films.³¹

The effect of CNT density on device performance is illustrated in Figure 4b, where the relevant device parameters (averaged over five devices) are plotted as a function of CNT density. The average width-normalized on-current (I_{on}/W , $I_{\text{on}} = I_d$ at $V_g = -2$ V) as well as average off-current of the devices ($W = 100 \mu\text{m}$) increases with CNT density. I_{on}/W increases by 2 orders of magnitude from density-1 to density-3 films and then increases only marginally ($\sim 30\%$) for density-4

CNT films. In contrast, I_{off} increases by only an order of magnitude for the first three CNT densities, but increases by more than 2 orders of magnitude for density-4 CNTs. These currents imply an almost constant on/off ratio up to density-3 and then more than 2 orders of magnitude decreased on/off ratio for density-4. In the lower part of Figure 4b, the subthreshold slope (SS) and drain voltage- and width-normalized transconductance ($g_{\text{m,nor}} = (1/(V_d W))(\partial I_d/\partial V_g)$ in the linear regime, $-2 \text{ V} < V_g < -1 \text{ V}$) are plotted as a function of CNT density. Note that the subthreshold slope remains close to 150 mV/decade up to density-3 films and then increases to 450 mV/decade for density-4 films. The normalized transconductance increases by 50 times from density-1 to density-3 and then increases by only 20% for density-4. The trade-off between on/off ratio and field-effect mobility indicated in Figure 4c reveals increasing μ up to density-3 without degradation in the on/off ratio. Further increases in CNT density result in decreased on/off ratio without a significant increase in field-effect mobility. This trade-off may reflect the significant role played by the

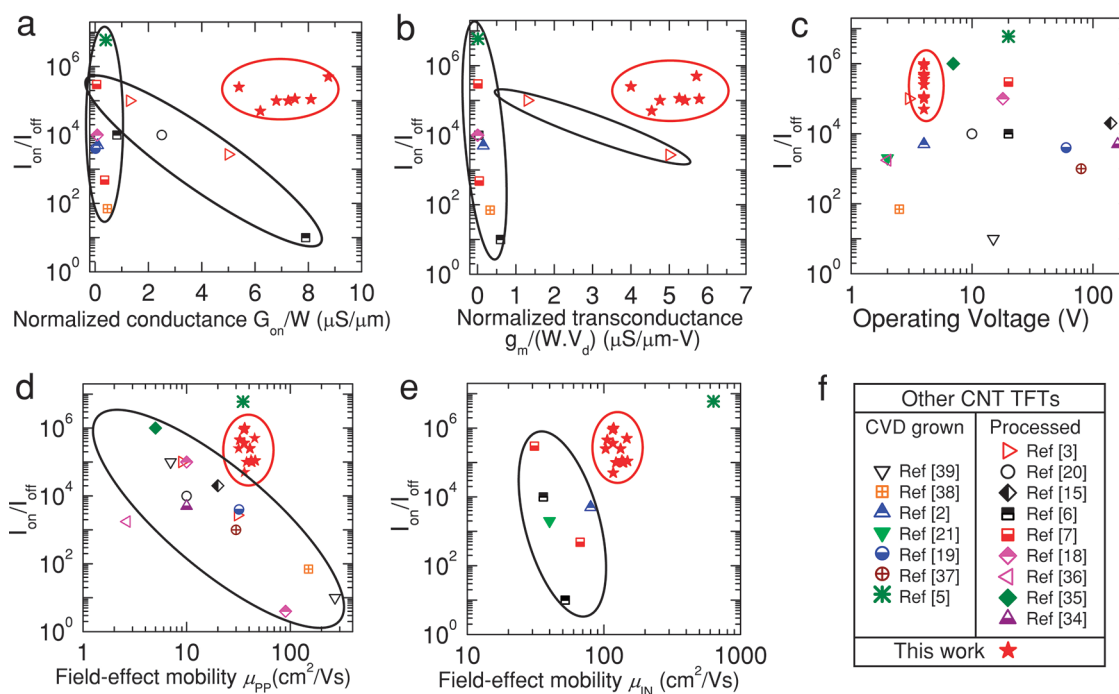


Figure 5. Comparison of CNT/VA-SAND TFT response with literature precedent. On/off ratio versus (a) on-state normalized conductance G_{on}/W , (b) normalized transconductance $g_m/(WV_d)$, and (c) operating voltage of density-3 (22.7 CNTs/ μm^2) CNT TFTs on VA-SAND ($L = 5 \mu\text{m}$, $W = 100 \mu\text{m}$), compared with device design trade-off trends for previously reported CNT TFTs. Plots of on/off ratio versus (d) parallel plate field-effect mobility μ_{pp} and (e) intrinsic field-effect mobility μ_{in} of density-3 CNT TFTs ($W = 100 \mu\text{m}$) on VA-SAND are compared with previously reported CNT TFTs. (f) Legend for previously reported CNT TFTs for all plots, a–e.

low fraction of metallic CNTs and/or the effects of CNT–CNT screening in thick monodisperse CNT films. Thus, integration of the hybrid VA-SAND gate dielectric with high-purity thick monodisperse CNTs allows optimization of device performance (density-3) to an average field-effect mobility of $\mu_{\text{pp}} = 42 \text{ cm}^2/(\text{V s})$ and $\mu_{\text{in}} = 136 \text{ cm}^2/(\text{V s})$ at an average on/off ratio of $\sim 10^5$. In contrast, as-grown CNTs produce low on/off ratios at significantly lower coverages due to the lower percolation threshold from the large fraction (30%) of long ($\sim 10 \mu\text{m}$) metallic CNTs,^{13,19} whereas monodisperse CNTs on low-capacitance gate dielectrics (e.g., 300 nm SiO_2) exhibit low on/off ratios, likely due to the onset of CNT–CNT screening at lower CNT densities.¹⁸

Density-3 CNT TFTs were further characterized to investigate large-area uniformity and channel geometry effects. The average transfer characteristics of seven density-3 CNT TFTs spread over $\sim 2 \text{ mm}$ in Figure 4d reveal excellent device-to-device uniformity. On-currents remain within $\pm 18\%$ and on/off ratios within 1 order of magnitude of the respective average values. Uniformity in such devices reflects the self-limiting thin-film growth mechanism of vacuum filtration.¹⁴ Note that a consistent TFT threshold voltage (within 100 mV of -0.5 V) is highly desirable for large-area low-voltage CNT circuitry. Figure 4g shows normalized on-state conductance ($G_{\text{on}}/W = G/W$ at $V_g = -2 \text{ V}$), intrinsic field-effect mobility (μ_{in}), and on/off ratio of density-3 CNT TFTs with L varying from 5 to $50 \mu\text{m}$ ($W = 100 \mu\text{m}$).

G_{on}/W decreases sharply with L , while the on/off ratio increases slightly with L . A slight fall in μ_{in} with L can be attributed to the sublinear length dependence of resistivity in percolating CNT networks, in agreement with previous reports.^{19,32}

We next examine the principal performance parameters of CNT/VA-SAND TFTs in the context of previously reported CNT TFT design trade-off relationships.^{2,3,5–7,15,18–21,34–39} Figure 5a–e show on/off ratios plotted as a function of normalized on-state conductance (G_{on}/W), normalized transconductance ($g_{m,\text{nor}}$), operating voltage, parallel-plate field-effect mobility (μ_{pp}), and intrinsic field-effect mobility (μ_{in}), respectively. A common legend for all the plots is shown in Figure 5f. Note that the transconductance data from the literature are also normalized with respect to the reported channel widths and drain biases. The best available performance parameters were extracted from the literature on random CVD-grown CNTs and solution-processed and purified semiconducting CNT TFTs and are then contrasted with optimized density-3 CNT/VA-SAND TFT data. Figure 5a–c show data for seven short channel length devices ($L = 5 \mu\text{m}$, $W = 100 \mu\text{m}$) taken from the transfer plots in Figure 4d. Figure 5d,e show data from all density-3 CNT TFTs, including devices with longer channel lengths from the transfer plots of Figure 4e. Although as-grown CNTs provide larger normalized conductance than monodisperse CNTs of the same network density, the metallic CNTs

in heterogeneous mixtures significantly erode on/off ratios.^{19,39} Note also that reduced on/off ratios result from high densities of monodisperse CNTs due to increased CNT–CNT screening.^{6,18} The present CNT films afford the highest normalized on-state conductance at an on/off ratio = 10^6 reported to date for CNT TFTs. The present random CNT/VA-SAND TFTs show larger on-state conductance at higher on/off ratios than ambipolar TFTs using thick CNT films on high-capacitance ion-gel dielectrics³ ($\sim 10 \mu\text{F}/\text{cm}^2$) and top-gated ambipolar TFTs having aligned monodisperse CNT strips.²⁰ P-type CNT TFTs show higher on/off ratios than ambipolar devices where both minority electrons and holes are present in the channel in the off-state, resulting in larger off-currents.⁴⁰ The present devices also exhibit significantly higher transconductance at an on/off ratio of $\sim 10^5$ due to the combined high-conductance and low-voltage operation (Figure 5c). As expected, there are no obvious trends in on/off ratio *versus* operating voltage in previously reported devices due to the large variations in operation strategies, device geometries, and gate-dielectric materials.

The trade-off between on/off ratio and field-effect mobility (Figures 5d,e) is similar to that of normalized on-state conductance and transconductance with larger (smaller) mobilities at lower (higher) on/off ratios. The present devices outperform the majority of the literature devices ($\mu_{\text{PP}} = 45 \text{ cm}^2/(\text{V s})$; $\mu_{\text{IN}} = 147 \text{ cm}^2/(\text{V s})$ at on/off ratio of 5×10^5) with comparable μ_{PP} and

lower μ_{IN} than high-quality CVD-grown CNT TFTs.⁵ Such devices exhibit high intrinsic mobility ($\sim 650 \text{ cm}^2/(\text{V s})$) due to the reduced intrinsic gate capacitance (C_{in} , Supporting Section 4) of a very sparse network of highly conductive long CNTs with possible covalent bonds at CNT–CNT junctions. Note however that the present devices show 100 times higher on-state conductance and transconductance and 5 times lower operating voltage with significantly reduced hysteresis and sub-threshold swing.

CONCLUSIONS

In summary, we have approached the fundamental performance limits for 99% purity semiconducting CNTs *via* integration with a high-capacitance hybrid inorganic–organic gate dielectric. Since the VA-SAND gate capacitance ($630 \text{ nF}/\text{cm}^2$) approaches the quantum capacitance of CNT films ($\sim 1 \mu\text{F}/\text{cm}^2$ for the density-3 CNT TFTs), further increases in gate capacitance may not yield significantly enhanced performance. Note that the performance reported here for CNT/VA-SAND TFTs compares favorably with devices fabricated from competing semiconducting materials such as polycrystalline Si,⁴¹ organics,⁴² and other inorganics.⁴³ The attractions of monodisperse semiconducting CNT inks include excellent compatibility with printing,³ mechanical flexibility, and environmental stability, making them promising candidates for next-generation printed electronics.

METHODS

VA-SAND Growth and Characterization. Twenty cycles of ALD-derived Al_2O_3 using trimethylaluminum and water as precursors were first grown on heavily doped n-Si (100) substrates at 100°C (Savannah, Cambridge NanoTech), followed by thermal evaporative deposition of the VA-SAND organic layer under high vacuum (10^{-6} Torr) at 25°C . Growth was carried out as described earlier,²¹ *i.e.*, at 0.1 – $0.2 \text{ \AA}/\text{s}$, to obtain a 3.4 nm thick bilayer of two head-to-tail hydrogen-bonded π -molecules. Finally, the organic layer was capped with an additional 20 cycles of an ALD-derived Al_2O_3 protective layer at 100°C . MIS capacitors were fabricated by thermal evaporation of 50 nm thick Au electrodes onto the dielectric layers through shadow masks. Leakage I – V measurements were carried out in ambient using a femto-amp Keithley source meter, and C – V measurements were made at 10 kHz using an HP 4192A impedance analyzer. The capacitances of VA-SAND and 6-AO are modeled as four and two parallel plate capacitors in series, respectively.

$$\frac{1}{C_{\text{VA-SAND}}} = \frac{1}{C_{\text{native-oxide}}} + \frac{1}{C_{\text{underlayer}}} + \frac{1}{C_{\text{chromophore}}} + \frac{1}{C_{\text{capping}}}$$

$$\frac{1}{C_{\text{6-AO}}} = \frac{1}{C_{\text{native-oxide}}} + \frac{1}{C_{\text{Al}_2\text{O}_3}}$$

$$C_i = \frac{\kappa_i \epsilon_0}{d_i}$$

where, C_i , κ_i , d_i , and ϵ_0 are capacitance per unit area, dielectric constant, thickness of the dielectric layer, and permittivity of

free space, respectively. The thickness of native oxide is found to be 1.8 nm by ellipsometry (J.A. Woolam Co. M2000 V VASE) on a blank substrate. The dielectric constant of ALD-grown Al_2O_3 was independently determined to be 6.0 from an MIS capacitor fabricated on 6 nm thick Al_2O_3 grown on a chemically etched Si substrate (without native oxide). The dielectric constant of the organic layer was previously determined as 9.5 by experiment and theoretical modeling.²⁴

X-ray Reflectivity Characterization of VA-SAND. XRR data were acquired using an 18 kW Rigaku ATXG diffractometer equipped with a Cu rotating anode ($\lambda = 1.541 \text{ \AA}$) equipped with a NaI scintillation detector. X-rays were conditioned with a multilayer parabolic mirror and collimated to $5.0 \text{ mm} \times 0.1 \text{ mm}$ (height \times width), yielding an incident beam flux of $\sim 1 \times 10^8$ at the sample surface.

CNT TFT Fabrication. Purification of 99% semiconducting arc-discharged CNTs was achieved by two iterations of DGU as described in detail in Supplementary Section 1.^{15–17} CNT films with four different network densities were prepared by vacuum filtration of 30, 60, 90, and $150 \mu\text{L}$ of 99% semiconducting CNT suspensions (diluted with 2 mL of 1% SC/DI H_2O) onto 1.42 cm^2 mixed cellulose ester membranes (Millipore, pore size = 50 nm). The self-limiting vacuum filtration process results in a uniform coating of the CNT film. The CNT films were then rinsed with 100 mL of DI H_2O to remove residual surfactant. Vacuum filtration affords large-area, clean, and uniform CNT films with excellent control over network density. The TFT source–drain electrodes (Cr/Au: $2/50 \text{ nm}$) were defined on VA-SAND by photolithography, thermal evaporation of the metals, and a lift-off process. An additional 15 nm thick Al_2O_3 film was grown by ALD on patterned photoresist before

electrode metallization to achieve robust electrical probing in a Cascade Microtech probe station (schematic in Figure 2d). CNT films were transferred onto patterned source–drain electrodes by dissolving the filter membranes in acetone vapor.¹⁷ The CNT films were then annealed in air at 225 °C for 1 h to further remove residual impurities. Finally, bottom-gate bottom-contact CNT TFT channels were defined using photolithography and reactive ion etching to obtain a channel width (W) of 100 μm and channel lengths (L) varying from 5 to 50 μm .

Conflict of Interest: The authors declare no competing financial interest.

Supporting Information Available: Density gradient ultracentrifugation of 99% semiconducting single-walled carbon nanotubes, length distribution of monodisperse CNTs, and calculations of field-effect mobility are provided. This material is available free of charge via the Internet at <http://pubs.acs.org>.

Author Contributions: M.C.H., T.J.M., L.J.L., and V.K.S. conceived the experiments and analyzed and interpreted data. R.P.O., J.M.P.A., and V.K.S. fabricated VA-SAND gate dielectrics. J.D.E. and M.J.B. conducted X-ray reflectivity experiments and analyzed data. V.K.S. fabricated the devices and conducted the measurements. All authors contributed to the discussion and writing of the manuscript.

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REFERENCES AND NOTES

- Jorio, A.; Dresselhaus, M. S.; Dresselhaus, G. *Advanced Topics in the Synthesis, Structure, Properties and Applications*; Springer: Berlin, 2008.
- Cao, Q.; Kim, H. S.; Pimparkar, N.; Kulkarni, J. P.; Wang, C. J.; Shim, M.; Roy, K.; Alam, M. A.; Rogers, J. A. Medium-Scale Carbon Nanotube Thin-Film Integrated Circuits on Flexible Plastic Substrates. *Nature* **2008**, *454*, 495–500.
- Ha, M.; Xia, Y.; Green, A. A.; Zhang, W.; Renn, M. J.; Kim, C. H.; Hersam, M. C.; Frisbie, C. D. Printed, Sub-3V Digital Circuits on Plastic from Aqueous Carbon Nanotube Inks. *ACS Nano* **2010**, *4*, 4388–4395.
- Kang, S. J.; Kocabas, C.; Ozel, T.; Shim, M.; Pimparkar, N.; Alam, M. A.; Rotkin, S. V.; Rogers, J. A. High-Performance Electronics Using Dense, Perfectly Aligned Arrays of Single-Walled Carbon Nanotubes. *Nat. Nanotechnol.* **2007**, *2*, 230–236.
- Sun, D.-M.; Timmermans, M. Y.; Tian, Y.; Nasibulin, A. G.; Kauppinen, E. I.; Kishimoto, S.; Mizutani, T.; Ohno, Y. Flexible High-Performance Carbon Nanotube Integrated Circuits. *Nat. Nanotechnol.* **2011**, *6*, 156–161.
- Wang, C.; Zhang, J.; Ryu, K.; Badmaev, A.; De Arco, L. G.; Zhou, C. Wafer-Scale Fabrication of Separated Carbon Nanotube Thin-Film Transistors for Display Applications. *Nano Lett.* **2009**, *9*, 4285–4291.
- Wang, C.; Zhang, J.; Zhou, C. Macroelectronic Integrated Circuits Using High-Performance Separated Carbon Nanotube Thin-Film Transistors. *ACS Nano* **2010**, *4*, 7123–7132.
- Nougaret, L.; Happy, H.; Dambrine, G.; Derycke, V.; Bourgoin, J. P.; Green, A. A.; Hersam, M. C. 80 GHz Field-Effect Transistors Produced Using High Purity Semiconducting Single-Walled Carbon Nanotubes. *Appl. Phys. Lett.* **2009**, *94*, 243505.
- Rutherglen, C.; Jain, D.; Burke, P. Nanotube Electronics for Radiofrequency Applications. *Nat. Nanotechnol.* **2009**, *4*, 811–819.
- Kinoshita, M.; Steiner, M.; Engel, M.; Small, J. P.; Green, A. A.; Hersam, M. C.; Krupke, R.; Mendez, E. E.; Avouris, P. The Polarized Carbon Nanotube Thin Film LED. *Opt. Express* **2010**, *18*, 25738–25745.
- Zhang, J.; Fu, Y.; Wang, C.; Chen, P.-C.; Liu, Z.; Wei, W.; Wu, C.; Thompson, M. E.; Zhou, C. Separated Carbon Nanotube Macroelectronics for Active Matrix Organic Light-Emitting Diode Displays. *Nano Lett.* **2011**, *11*, 4852–4858.
- Cao, Q.; Rogers, J. A. Ultrathin Films of Single-Walled Carbon Nanotubes for Electronics and Sensors: A Review of Fundamental and Applied Aspects. *Adv. Mater.* **2009**, *21*, 29–53.
- Rouhi, N.; Jain, D.; Burke, P. J. High-Performance Semiconducting Nanotube Inks: Progress and Prospects. *ACS Nano* **2011**, *5*, 8471–8487.
- Wu, Z. C.; Chen, Z. H.; Du, X.; Logan, J. M.; Sippel, J.; Nikolou, M.; Kamaras, K.; Reynolds, J. R.; Tanner, D. B.; Hebard, A. F.; et al. Transparent, Conductive Carbon Nanotube Films. *Science* **2004**, *305*, 1273–1276.
- Arnold, M. S.; Green, A. A.; Hulvat, J. F.; Stupp, S. I.; Hersam, M. C. Sorting Carbon Nanotubes by Electronic Structure Using Density Differentiation. *Nat. Nanotechnol.* **2006**, *1*, 60–65.
- Arnold, M. S.; Stupp, S. I.; Hersam, M. C. Enrichment of Single-Walled Carbon Nanotubes by Diameter in Density Gradients. *Nano Lett.* **2005**, *5*, 713–718.
- Green, A. A.; Hersam, M. C. Nearly Single-Chirality Single-Walled Carbon Nanotubes Produced via Orthogonal Iterative Density Gradient Ultracentrifugation. *Adv. Mater.* **2011**, *23*, 2185–2190.
- Rouhi, N.; Jain, D.; Zand, K.; Burke, P. J. Fundamental Limits on the Mobility of Nanotube-Based Semiconducting Inks. *Adv. Mater.* **2011**, *23*, 94–99.
- Sangwan, V. K.; Behnam, A.; Ballarotto, V. W.; Fuhrer, M. S.; Ural, A.; Williams, E. D. Optimizing Transistor Performance of Percolating Carbon Nanotube Networks. *Appl. Phys. Lett.* **2010**, *97*, 043111.
- Engel, M.; Small, J. P.; Steiner, M.; Freitag, M.; Green, A. A.; Hersam, M. C.; Avouris, P. Thin Film Nanotube Transistors Based on Self-Assembled, Aligned, Semiconducting Carbon Nanotube Arrays. *ACS Nano* **2008**, *2*, 2445–2452.
- Cao, Q.; Xia, M. G.; Shim, M.; Rogers, J. A. Bilayer Organic–Inorganic Gate Dielectrics for High-Performance, Low-Voltage, Single-Walled Carbon Nanotube Thin-Film Transistors, Complementary Logic Gates, and p–n Diodes on Plastic Substrates. *Adv. Funct. Mater.* **2006**, *16*, 2355–2362.
- Hur, S.-H.; Yoon, M.-H.; Gaur, A.; Shim, M.; Facchetti, A.; Marks, T. J.; Rogers, J. A. Organic Nanodielectrics for Low Voltage Carbon Nanotube Thin Film Transistors and Complementary Logic Gates. *J. Am. Chem. Soc.* **2005**, *127*, 13808–13809.
- DiBenedetto, S. A.; Facchetti, A.; Ratner, M. A.; Marks, T. J. Molecular Self-Assembled Monolayers and Multilayers for Organic and Unconventional Inorganic Thin-Film Transistor Applications. *Adv. Mater.* **2009**, *21*, 1407–1433.
- DiBenedetto, S. A.; Frattarelli, D.; Ratner, M. A.; Facchetti, A.; Marks, T. J. Vapor Phase Self-Assembly of Molecular Gate Dielectrics for Thin Film Transistors. *J. Am. Chem. Soc.* **2008**, *130*, 7528–7529.
- Nelson, A. Co-refinement of Multiple-Contrast Neutron/X-ray Reflectivity Data Using MOTOFIT. *J. Appl. Crystallogr.* **2006**, *39*, 273–276.
- Fukuto, M.; Heilmann, R. K.; Pershan, P. S.; Yu, S. M.; Soto, C. M.; Tirrell, D. A. Internal Segregation and Side Chain Ordering in Hairy-Rod Polypeptide Monolayers at the Gas/Water Interface: An X-ray Scattering Study. *J. Chem. Phys.* **2003**, *119*, 6253–6270.
- Durkop, T.; Getty, S. A.; Cobas, E.; Fuhrer, M. S. Extraordinary Mobility in Semiconducting Carbon Nanotubes. *Nano Lett.* **2004**, *4*, 35–39.
- Cao, Q.; Xia, M.; Kocabas, C.; Shim, M.; Rogers, J. A.; Rotkin, S. V. Gate Capacitance Coupling of Singled-Walled Carbon

- Nanotube Thin-Film Transistors. *Appl. Phys. Lett.* **2007**, *90*, 023516.
29. Kocabas, C.; Pimparkar, N.; Yesilyurt, O.; Kang, S. J.; Alam, M. A.; Rogers, J. A. Experimental and Theoretical Studies of Transport through Large Scale, Partially Aligned Arrays of Single-Walled Carbon Nanotubes in Thin Film Type Transistors. *Nano Lett.* **2007**, *7*, 1195–1202.
 30. Appenzeller, J.; Lin, Y. M.; Knoch, J.; Avouris, P. Band-to-Band Tunneling in Carbon Nanotube Field-Effect Transistors. *Phys. Rev. Lett.* **2004**, *93*.
 31. Kim, W.; Javey, A.; Vermesh, O.; Wang, O.; Li, Y. M.; Dai, H. J. Hysteresis Caused by Water Molecules in Carbon Nanotube Field-Effect Transistors. *Nano Lett.* **2003**, *3*, 193–198.
 32. Kumar, S.; Murthy, J. Y.; Alam, M. A. Percolating Conduction in Finite Nanotube Networks. *Phys. Rev. Lett.* **2005**, *95*, 066802.
 33. Izard, N.; Kazaoui, S.; Hata, K.; Okazaki, T.; Saito, T.; Iijima, S.; Minami, N. Semiconductor-Enriched Single Wall Carbon Nanotube Networks Applied to Field Effect Transistors. *Appl. Phys. Lett.* **2008**, *92*, 243112.
 34. Lee, C. W.; Han, X.; Chen, F.; Wei, J.; Chen, Y.; Chan-Park, M. B.; Li, L.-J. Solution-Processable Carbon Nanotubes for Semiconducting Thin-Film Transistor Devices. *Adv. Mater.* **2010**, *22*, 1278–1282.
 35. LeMieux, M. C.; Roberts, M.; Barman, S.; Jin, Y. W.; Kim, J. M.; Bao, Z. Self-Sorted, Aligned Nanotube Networks for Thin-Film Transistors. *Science* **2008**, *321*, 101–104.
 36. Roberts, M. E.; LeMieux, M. C.; Sokolov, A. N.; Bao, Z. Self-Sorted Nanotube Networks on Polymer Dielectrics for Low-Voltage Thin-Film Transistors. *Nano Lett.* **2009**, *9*, 2526–2531.
 37. Sangwan, V. K.; Southard, A.; Moore, T. L.; Ballarotto, V. W.; Hines, D. R.; Fuhrer, M. S.; Williams, E. D. Transfer Printing Approach to All-Carbon Nanoelectronics. *Microelectron. Eng.* **2011**, *88*, 3150–3154.
 38. Snow, E. S.; Campbell, P. M.; Ancona, M. G.; Novak, J. P. High-Mobility Carbon-Nanotube Thin-Film Transistors on a Polymeric Substrate. *Appl. Phys. Lett.* **2005**, *86*, 033105.
 39. Snow, E. S.; Novak, J. P.; Campbell, P. M.; Park, D. Random Networks of Carbon Nanotubes as an Electronic Material. *Appl. Phys. Lett.* **2003**, *82*, 2145–2147.
 40. Martel, R.; Derycke, V.; Lavoie, C.; Appenzeller, J.; Chan, K. K.; Tersoff, J.; Avouris, P. Ambipolar Electrical Transport in Semiconducting Single-Wall Carbon Nanotubes. *Phys. Rev. Lett.* **2001**, *87*, 256805.
 41. Pecora, A.; Maiolo, L.; Cuscunà, M.; Simeone, D.; Minotti, A.; Mariucci, L.; Fortunato, G. Low-Temperature Polysilicon Thin Film Transistors on Polyimide Substrates for Electronics on Plastic. *Solid-State Electron.* **2008**, *52*, 348–352.
 42. Forrest, S. R. The Path to Ubiquitous and Low-Cost Organic Electronic Appliances on Plastic. *Nature* **2004**, *428*, 911–918.
 43. Kim, M.; Jeong, J. H.; Lee, H. J.; Ahn, T. K.; Shin, H. S.; Park, J.-S.; Jeong, J. K.; Mo, Y.-G.; Kim, H. D. High Mobility Bottom Gate InGaZnO Thin Film Transistors with SiO_x Etch Stopper. *Appl. Phys. Lett.* **2007**, *90*, 212114.